

ABSTRACT

A method and computer for executing the method. A binary translator is programmed to translate at least a segment of a binary representation of a program from a first representation in a first instruction set architecture to a second representation in a second instruction set architecture. A sequence of side-effects in the second representation differs from a sequence of side-effects in the translated segment of the first representation. The second representation distinguishes individual memory loads that are believed to be directed to well-behaved memory from memory loads that are believed to be directed to non-well-behaved memory device(s). Instruction execution circuitry identifies an individual memory-reference instruction in the second representation, or an individual memory reference of an instruction, a side-effect arising from the memory reference having been reordered by the translator, the memory reference having been believed at translation time to be directed to well-behaved memory but that at execution found to references a device with a valid memory address that cannot be guaranteed to be well-behaved. Based in the distinguishing, the instruction execution circuitry identifies whether the difference in sequence of side-effects may have a material effect on the execution of the program. Circuitry and/or software establishes a program state to a state equivalent to a state that would have occurred in the execution of the first representation, and resumes execution of the translated segment of the program in the first instruction set.